EXPRESS MAIL LABEL NO. EV381146341US
DATE MAILED: April 1, 2004

PATENT

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METHOD OF FABRICATING A SEMICONDUCTOR DEVICE COMPRISING A GATE DIELECTRIC MADE OF HIGH DIELECTRIC PERMITTIVITY MATERIAL

Cross-Reference To Related Applications

[001] This application is based upon and claims priority from prior French Patent Application No. 03 04008, filed on April 1, 2003 the entire disclosure of which is herein incorporated by reference.

Field of the Invention

[002] The present invention relates to a method of fabricating a semiconductor device comprising a gate dielectric made of high dielectric permittivity material and to a semiconductor device such as an MOS and CMOS transistor obtained by this process.

Background of the Invention

[003] The material generally used to form the gate of an MOS transistor, in particular in the case of short-channel transistors (channel length less than 0.18 μm) is polycrystalline silicon (poly-silicon or poly-Si). Conventionally, the gates of these transistors are obtained by high-density plasma etching of a poly-Si layer deposited on a thin layer of dielectric (gate dielectric), typically made of silicon oxide (SiO_2), formed on the surface of a single-crystal silicon substrate.

[004] At the present time it is sought to replace the SiO_2 layer with a layer of a dielectric having a high dielectric permittivity (high-k material) for low-energy-

consumption applications requiring a low leakage current. The introduction of high-k materials for the purpose of replacing SiO_2 must firstly be accomplished with a standard poly-Si gate.

[005] In recent years, attempts have been made to develop high-k material as much as the poly-Si gate. It seems that the metal-oxide-type materials investigated hitherto are incompatible with a standard poly-Si gate deposition process. On this subject, the reader may refer to the article *"Compatibility of Polycrystalline Silicon Gate Deposition with HfO_2 and HfO_2/Al_2O_3 Gate Dielectrics"* by D.C. Gilmer et al., MOTOROLA (APL, Vol. 81, No 7, pp 1288-1290). This is because a large number of short-circuit-type defects are generated, of the order of 10^4 defects per cm^2.

[006] From studies and observations made by the inventors, which are the basis of the present invention, it is considered that the appearance of these defects is probably due to direct interaction between, on the one hand, the gases used during deposition of the poly-Si gate, namely silane (SiH_4) and hydrogen (H_2), and, on the other hand, the surface of the high-k material, owing to the high temperature, of around, but not limited to, 550°C, at which this deposition is carried out. When the high-k material is a layer of hafnium oxide (HfO_2), the interaction in this case is an Hf/Si-type interaction that occurs at temperatures of around, but not limited to, 550°C or higher.

[007] To alleviate this problem, two approaches are in principle conceivable: the first would be to modify the high-k material and the second would be to modify the gate.

[008] Regarding the first approach, it is known that many studies have been carried out in order to modify the high-k material, but this generally results either in a reduction in the dielectric permittivity (k) or in an increase in the number of fixed charges in the material, having the effect of degrading the characteristics of the transistors. On this subject, the reader may refer to the article "*Effect of Nitrogen in HfSiON Gate Dielectrics on the Electrical and Thermal*

Characteristics" M. Koyoma et al., Toshiba Corporation (IEDM 2002), which is hereby incorporated by reference in its entitety.

[009] As regards the second approach, it is also known that the use of a metallic gate, especially a gate made of titanium nitride (TiN), does admittedly avoid the problem of generating defects, but it poses many problems of integration and of compatibility with an FEOL (Front-End Of the Line) process. In particular, it is preferable to maintain a poly-Si gate that offers the possibility of n-doping or p-doping by ion implantation.

[010] Moreover, EP-A1-0 887 843 teaches a transistor having a Si/SiGe composite gate, that comprises a SiO_2 layer on a Si semiconductor substrate, a Si tie layer with a thickness of less than or equal to 1 nm on the SiO_2 layer, and a polycrystalline $Si_{1-x}Ge_x$ layer, where $0 < x \leq y$, with a thickness of around, but not limited to, 2 to 20 nm, on this tie layer, the $Si_{1-x}Ge_x$ being surmounted by a Si layer. The tie layer is deposited at a temperature of between 500 and 580°C, typically 550°C. This is why the aforementioned interactions of the Hf-Si type would occur at the interface with the layer of high-k material if such a layer were to replace the SiO_2 layer.

[011] According what is needed is a method and system to over come the problems encountered in the prior art and to provide a transistor gate that is less aggressive with respect to the high-k material in the first steps of depositing the gate, but that is also compatible with the conventional fabrication processes, especially including the adjustment of the gate work function by ion implantation.

Summary of the Invention

[012] Briefly, in accordance with a first aspect of the present invention relates to a method of fabricating a semiconductor device having a gate dielectric made of high dielectric permittivity material, that includes a step of depositing, directly on the gate dielectric, a $Si_{1-x}Ge_x$ first layer, where $0.5 < x \leq 1$, at a temperature substantially below the temperature at which the poly-Si is deposited by thermal CVD.

[013] The method, in one embodiment, furthermore includes a step of depositing a $Si_{1-y}Ge_y$ second layer, where $0 \leq y \leq 1$, on top of the $Si_{1-x}Ge_x$ first layer.

[014] A second aspect of the present invention relates to a semiconductor device comprising, on a substrate, a gate dielectric made of high dielectric permittivity material and, on top of the gate dielectric, a gate comprising a $Si_{1-x}Ge_x$ first layer, where $0.5 < x \leq 1$, directly on the gate dielectric.

[015] Thus, the present invention uses $Si_{1-x}Ge_x$, where $0.5 < x \leq 1$, for the first deposition step carried out directly on the high-k material, during production of the gate, so as to stabilize the interface between the high-k material and the gate, without degrading the high-k material. Once this interface has been established, the conventional process for producing the poly-Si gate is then continued, with the associated thermal budgets.

Brief Description of the Drawings

[016] The subject matter, which is regarded as the invention, is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other features, and advantages of the invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[017] FIGs. 1 to 5 are schematic sectional views illustrating an example of a semiconductor device according to the main steps of the method of forming the gate on top of a layer of high-k material in accordance with the present invention; and

[018] FIG. 6 is a diagram of the steps illustrating an example of a method according to the present invention.

Description Of The Preferred Embodiments

[019] It should be understood that these embodiments are only examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily limit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others. In general, unless otherwise indicated, singular elements may be in the plural and vice versa with no loss of generality.

[020] The device here is, for example, the gate of an MOS transistor, which is a particular case of a capacitor plate. However, it is quite clear that the invention is not limited to this example, rather it applies to the production of any semiconductor device comprising a gate dielectric made of high-k dielectric.

[021] FIGs. 1 to 5 show, in cross section, that portion of a silicon substrate 1 that corresponds to an active zone for producing the gate of the MOS transistor. The active zone is, for example, part of a p-doped native substrate, in order to produce an n-channel MOS transistor (nMOS transistor). To produce a p-channel MOS transistor (pMOS transistor), the active zone is, for example, an n-doped well in a p-doped native substrate.

[022] FIG. 6 illustrates the steps of an example of how the present invention is carried out.

[023] Applications of the invention are, in particular, in the fabrication of MOS transistors in CMOS technology or the like.

[024] Starting from a native silicon substrate, the first step 10 consists in defining at least one active zone as illustrated in FIG. 1.

[025] The second step 20 consists in preparing the surface of the substrate, in the active zone, for the purpose of depositing the high-k dielectric. In one embodiment, this step includes the formation of a very thin layer of gate oxide, made of SiO_2 or the like (SiON, etc).

[026] FIG. 2 illustrates the third step 30 of producing the gate oxide layer on the surface of the substrate 1 by depositing a high-k-type dielectric, for example HfO_2. This step comprises:

[027] the formation of an oxide layer, having a thickness of about, but not limited to, 0.7 nm, by ozone chemistry;

[028] the deposition of an HfO_2 layer, having a thickness of about, but not limited to, 4 nm, for example by ALCVD (Atomic Layer Chemical Vapor Deposition) at a temperature of around, but not limited to, 300°C ; and

[029] an annealing operation at about, but not limited to, 600°C in the presence of nitrogen (N_2) for about, but not limited to, 1 minute.

[030] A gate oxide layer 2 made of crystallized HfO_2 is thus obtained.

[031] It shall be noted that other dielectrics of the metal oxide type are encompassed within the true scope and spirit of the present invention, for example other metal oxides such as zirconium oxide (ZrO_2), hafnium silicate (HfSiO) and zirconium silicate (ZrSiO).

[032] Steps 10, 20 and 30 are indicated here, according to one example of how to carry out the process, for the sake of clarity of the description. However, it is quite obvious that these are not themselves constitutive of the process according to the present invention.

[033] In the fourth step 40 illustrated in FIG. 3, a layer 3 of polycrystalline $Si_{1-x}Ge_x$, where $0.5 < x \leq 1$, is then deposited at low temperature directly on the gate oxide layer 2.

[034] The term "low temperature" is understood, here and below, to mean a temperature substantially below the temperature of Si deposition by thermal CVD (Chemical Vapor Deposition) using a SiH_4/H_2 gas mixture, this temperature being in general equal to 550°C or higher.

[035] Preferably, the layer 3 in one embodiment is deposited at a temperature between 400 and 500°C, or better still between 400 and 450°C. It has been observed that, at such a temperature, degradation of the high-k material is avoided.

[036] In a first implementation example, the deposition is carried out in this step 40 by thermal CVD using a gas mixture containing SiH_4 and/or GeH_4 diluted in H_2, typically to 10%.

[037] In this case, it is preferable for $0.7 \leq x \leq 1$. This is because the higher the Ge content, the lower the deposition temperature may be. Thus, to deposit a layer of pure Ge (x=1), the temperature may be approximately 400 °C.

[038] This deposition is less aggressive than deposition by thermal CVD based on SiH_4 diluted in H_2, which typically is carried out with a thermal budget of 550°C. The interface between the high-k material and the gate is therefore stabilized without degrading this material.

[039] The proportions of the various gases of the gas mixture for the $Si_{1-x}Ge_x$ layer vary according to x and may be easily determined by those of average skill in the art on the basis of the Ge and Si contents desired for this layer.

[040] The total deposition pressure is generally a low pressure, that is to say below atmospheric pressure.

[041] The duration of the deposition depends on the temperature and pressure conditions, on the proportions of the various gases in the gas mixture and on the desired thickness of the polycrystalline $Si_{1-x}Ge_x$ layer 3. For example, the thickness of this layer is between 5 and 30 nm.

[042] Advantageously, since the Ge content of the gate is high (x>0.5), the poly-depletion of the gate is greatly improved. In this regard, reference may be made to the article "*Enhancement of PMOS Device Performance with Poly-SiGe Gate*", by Wen-Chin Lee et al., IEEE (EDL 1999, Vol. 20, No. 5, pp 232-234).

[043] In the fifth step 50 illustrated in FIG. 4, a second layer 4, for example made of poly-Si, is then deposited on top of the layer 3 so as to complete the thickness of the gate to about, but not limited to, 150 nm in total.

[044] It should be noted that the deposition in this step 50 does not need to be carried out at low temperature (in the sense indicated above), since the interface between the layer of high-k material and the $Si_{1-x}Ge_x$ first layer, that is to say between the layer 2 and the layer 3, has already stabilized. There is therefore no possible interaction of the Hf/Si type.

[045] As a variant, the layer 4 may be made of polycrystalline $Si_{1-y}Ge_y$, where $0 \leq y \leq 1$.

[046] This step 50 may advantageously be carried out in the same reactor as step 40. As required, only the gas mixture is different.

[047] In the sixth step 60, which is optional, a diffusion annealing operation may be carried out in order to obtain interdiffusion of the Ge and/or Si between the layers 3 and 4, that is to say diffusion of the Ge and/or of the Si of the layer 3 into the layer 4 and/or, conversely, of the layer 4 into the layer 3. This step is beneficial, in particular if the layer 3 is predominantly Ge, or even pure Ge, and/or if the layer 4 is predominantly Si, or even pure Si.

[048] This annealing operation therefore makes it possible to obtain a gate of the polycrystalline SiGe type.

[049] By correctly choosing the annealing parameters, especially the time and the temperature, it is advantageously possible to obtain an interface between the high-k material and the gate (interface between the layers 2 and 3) that is predominantly Si. In this way, the mid-gap gate effect due to p^+-doped pure Ge is avoided. A compromise may be found so as to maintain the advantage resulting from the presence of Ge as regards poly-depletion.

[050] Alternatively, it is also possible to form a layer 5 that limits the interdiffusion of Ge and Si, this layer being deposited between the layers 3 and 4,

so as to limit the diffusion of Ge and of Si from one of these layers into the other, and vice versa, during the subsequent annealing operations. The layer 5 is, for example, a superficial layer of silicon nitride or silicon oxide with a thickness of less than or equal to 1 nm. A process for obtaining such a layer is described for example in Patent Application FR-A-2 775 119. The configuration illustrated in FIG. 5 is then obtained.

[051] Finally, in the next steps, the other steps in the production of the MOS transistor according to the standard process are completed. These other steps include etching of the gate and production of the spacer around the gate (with deposition and optionally removal of the masks needed for this purpose). The next steps may also include the implantation of the n^+ or p^+ dopants for applications in CMOS technology, and their activation by annealing.

[052] According to one advantage of the present invention, the polycrystalline SiGe (poly-SiGe) gate may thus be treated as a standard poly-Si gate in order to adjust the gate work function by ion implantation.

[053] Optionally, an encapsulation layer may be added to the gate, covering the layer 3 and/or the layer 4, so as to protect the germanium from oxidation and from possible evaporation of its oxide. This encapsulation layer may be of SiO_2, and obtained using a standard deposition process.

[054] In pMOS and nMOS applications, the layer 3 and/or the layer 4 may be doped *in situ* as p^+ with boron (B) atoms or as n^+ with phosphorus (P) atoms respectively. The expression "*in situ* doping" is understood to mean doping in the presence of dopants in the gas mixture used to deposit the layer in question. For this purpose, it is sufficient to add phosphine (PH_3), or alternatively diborane (B_2H_6), to the gas mixture used for depositing these layers by thermal CVD (first implementation example for the layer 3).

[055] *In situ* doping is recommended when a layer for limiting the interdiffusion of Ge and Si, as mentioned above, is provided. Specifically, the layer may form a barrier to the diffusion of the dopants into the interface between the layers 2 and 3.

[056] The present invention has been described above in the case of a general implementation example that is not limiting.

[057] In a one particular implementation example, a provision is made for the layer 3 and the layer 4 to be both SiGe compounds having a high Ge content, for example greater than 70%, i.e. $Si_{1-x}Ge_x$ where $0.7 < x \leq 1$. This allows better control of the Ge concentration in the final gate.

[058] In another implementation example, Ge may be the only material of the gate. In other words, the layers 3 and 4 are then made of pure Ge (x=1). This may be advantageous in the context of a complete process by thermal CVD with a low thermal budget.

[059] Although a specific embodiment of the present invention has been disclosed, it will be understood by those having skill in the art that changes can be made to this specific embodiment without departing from the spirit and scope of the present invention. The scope of the present invention is not to be restricted, therefore, to the specific embodiment, and it is intended that the appended claims cover any and all such applications, modifications, and embodiments within the scope of the present invention.

[060] What is claimed is: